

December 15, 2003

To: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/666,359 09/19/03

Chi-Chun Chen et al.

METHOD OF FORMING AN ULTRATHIN NITRIDE/OXIDE STACK AS A GATE DIELECTRIC

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December) $^{\circ}$, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

TSMC-01-1488

- U.S. Patent 6,228,779 to Bloom et al., "Ultra Thin
 Oxynitride and Nitride/Oxide Stacked Gate Dielectrics
 Fabricated by High Pressure Technology," describes an SiON and
 ON stack gate dielectric high pressure process.
- U.S. Patent 6,017,791 to Wang et al., "Multi-Layer Silicon Nitride Deposition Method for Forming Low Oxidation Temperature Thermally Oxidized Silicon Nitride/Silicon Oxide (NO) Layer," describes an ON process for a gate dielectric.
- U.S. Patent 6,020,238 to He et al., "Method of Fabricating a High Dielectric Constant Interpolysilicon Dielectric Structure for a Low Voltage Non-Volatile Memory", describes a high-k (high dielectric constant) gate dielectric process for a low voltage non-volatile memory.
- U.S. Patent 5,464,792 to Tseng et al., "Process to Incorporate Nitrogen at an Interface of a Dielectric Layer in a Semiconductor Device," describes a process to incorporate nitrogen at an interface of a dielectric layer in a semiconductor device.

Sincerely

Stephen B. Ackerman, Reg. No. 37761

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citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.